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Hardware Design Guidelines
for POWERLINK SLAVE on FPGA

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I Versions

Version	Date	Comment	Edited by
0.1.0	Aug 13, 2010	Document creation	Zelenka Joerg
0.1.1	Sep 16, 2010	Timing Specification of Asynchronous 8/16bit MCU Interface and SPI	Zelenka Joerg
0.1.2	Nov 16, 2010	Added GPIO pins to Asynchronous 8/16bit MCU Interface Added OP pin to Digital I/O Interface	Zelenka Joerg
0.1.3	Dec 7, 2010	Added GPIO pins to SPI Interface	Zelenka Joerg
0.1.4	Mar 1, 2011	Added Part Nr. of recommended Parts	Michael Hogger
0.1.5	Mar 25, 2011	Revise Asynchronous 8/16bit MCU Interface	Zelenka Joerg
0.1.6	Apr 4, 2011	Revise Asynchronous 8/16 bit MCU Interface	Zelenka Joerg
0.1.7	Apr 20, 2011	Added Timing Specification of Digital I/O Latch functionality	Zelenka Joerg
0.2.0	Mai 07,2012	Add additional FPGA vendor information	Thomas Mair
0.2.1	May 15, 2012	Revised recommended Parts	Zelenka Joerg

Table 1: Versions

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1 Hardware Requirements

1.1 Design Overview

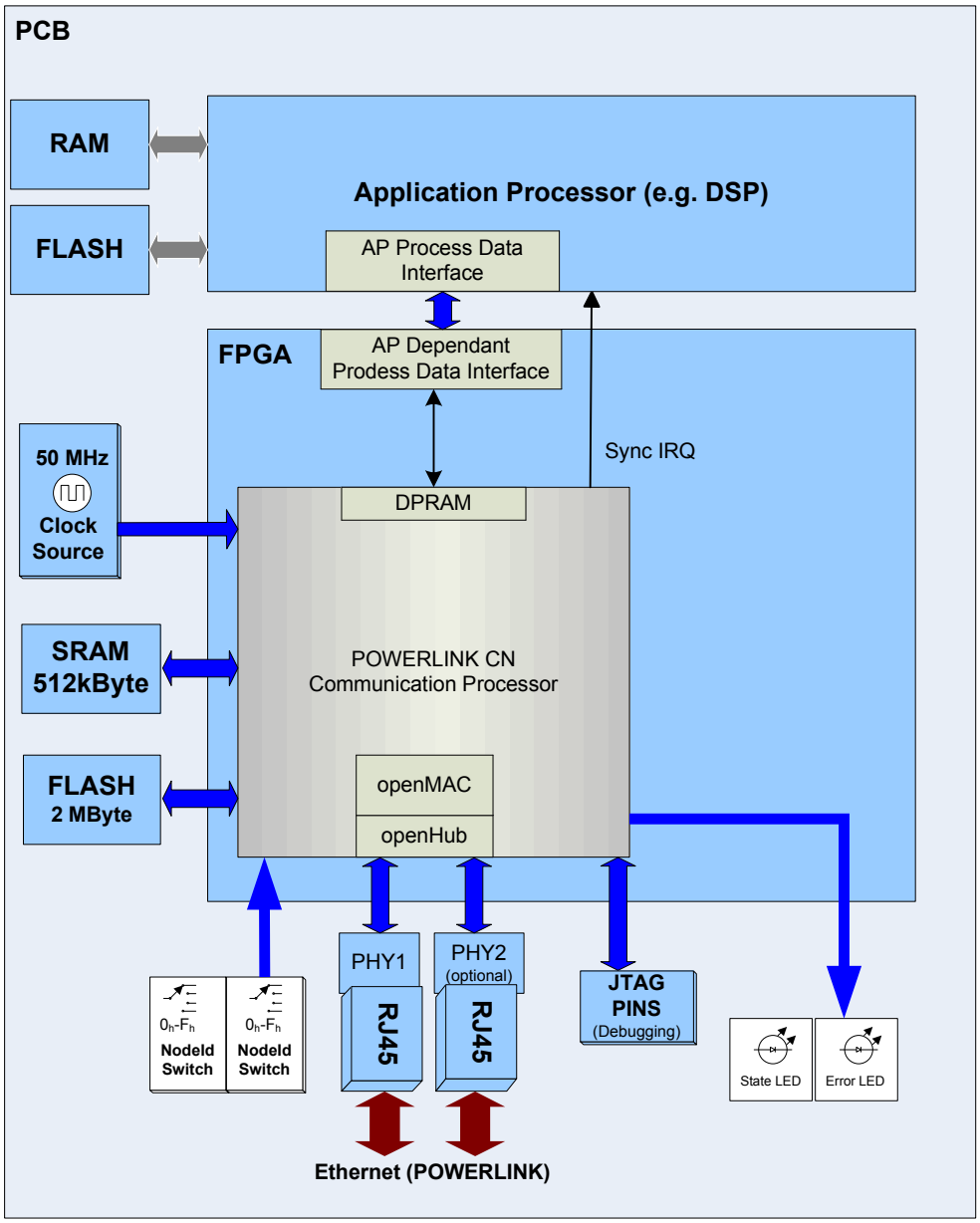

Fig. 1: Overview of Full Featured POWERLINK CN HW Design

For a full featured POWERLINK CN solution the design should look like the above depicted. The block diagram shows the necessary hardware modules with additionally included soft cores. These modules are further described in this chapter.

1.2 Design Reference

The **Avnet Spartan-6 LX16 - Powerlink Evaluation Board (s6plkeb)** serves as evaluation platform and design reference. Your design may vary from the evaluation board design due to economical or performance considerations. Nevertheless, general recommendations can be found in this user guide.

The evaluation board can be purchased via Avnet Asia at:
http://www.em.avnetasia.com/Products/DesignSolutionShow.aspx?pagesId=27&MasterPageId=17&ID=39 (2012-05-07)

All HW parts on this board are conventional. Thus, no special silicon IC's are required for implementing POWERLINK on FPGA. Please be aware that this design provides only the FPGA part with its peripherals. There is no second external processor placed on this evaluation board.

It is recommended to use the evaluation board schematics as a reference for your HW design. Several sections in this document directly refer to those schematics.
The schematics, bill of material and board views are included in the reference document [1].

1.3 FPGA

Design Recommendation for PCP with external MCU interface	
FPGA Device	**Xilinx Spartan 6**
Type	**XC6SLX9 up to XC6SLX45**
Recommended Part	**XC6SLX16**

The POWERLINK slave design utilizes a Xilinx Spartan 6 FPGA. In order to successfully fit in the design (with application specific addition) an XC6SLX16 should be used. This device provides about 14k logical elements, 136kByte on-chip memory and 232 user I/O pins. In some applications where an internal packet buffer is sufficient the use of an XC6LX9 is also possible.

Xilinx provides an overview of the different Spartan 6 FPGAs at:
http://www.xilinx.com/support/documentation/data_sheets/ds160.pdf

The reference HW design is shown with a Xilinx Spartan 6 XC6SLX16 FPGA schematic. [1] In this document all components are necessary except if the application processor is externally only one RAM is needed.

Furthermore the power supply of the FPGA is also shown in [1] on page 7. This schematic shows some DC/DC converters; however a detailed user guide for Spartan 6 FPGA's is available on:
http://www.xilinx.com/support/documentation/data_sheets/ds162.pdf

1.4 Volatile Memory

1.4.1 SRAM

Design Recommendation for PCP with external MCU interface	
Type of memory	**SRAM**
Minimum size	**512kByte**
Data Width	**16 or 32 Bit**
Performance	**10ns**
Recommended Part	• **CY7C1041DV33-10BVXIT** • **IS61WV25616BLL-10BLI**

The soft core Microblaze® executes the openPOWERLINK stack + application out of external RAM. In order to provide high performance the requirements shown above should be satisfied.

Information:

If one single 32 Bit or two 16 Bit SRAMs are being used it will increase the performance. A proper embedded memory controller is provided by Xilinx. (axi/plb_emc)

The reference HW design for an SRAM (CY7C1041DV33) is shown with a Spartan 6 XC6SLX16 FPGA in [1] on page 3.

1.4.2 DDRX

As Spartan 6 FPGA's provide a hardcoded memory controller it is also possible to use a DDRX RAM. The DDRX memory controller from Xilinx is connected to a 650Mhz clock source and therefore provides a rather good throughput and access latency. Still it is recommended to put the TX packets of the POWERLINK IP-Core into internal BRAM memory as the indeterministic characteristic of a DRAM can produce a long access latency which can result in a malformed TX packet. The IP-Core provides a DMA monitor circuit which produces an error before malformed POWERLINK packets are sent throughout the network.

The reference HW design for a DDR2 RAM (MT47H128M16) is shown with a Spartan 6 XC6SLX16 FPGA in [1] on page 4.

1.5 Non-Volatile Memory

Design Recommendation for PCP with external MCU interface	
Type of memory	serial FLASH with SPI interface
Size	16 Megabit
Recommended Part	S25FL016P 16-Mbit CMOS 3.0 Volt Flash Memory

Information:

If you use a bigger FPGA than XC6SLX16, you might increase the size of the serial FLASH memory!

The FPGA configuration data and the software for the soft core CPU can be stored within one non-volatile storage device. Xilinx provides serial flash components, which configure the FPGA after power up.
The flash memory size depends on the used FPGA (e.g. XC6SLX16 or XC6SLX45), the openPOWERLINK slave code size of 200kB and the node application itself.

The total size of the FPGA configuration data and the code (openPOWERLINK stack + application) must be stored in the FLASH. Furthermore the ability of remote update functionality has to be considered. Thus the total size needs to be multiplied by the different images.

Example:

In order to clarify the calculation of the flash-size the following example is assumed:
The used FPGA is a Xilinx Spartan 6 XC6SLX16, which needs 3,731,264 Bits = 467kB.
The Microblaze software code size (openPOWERLINK + application) is approximately 250kB.
In total two different images are used (one factory image and one user image).
flashSize = (FPGAdataSize + SoftwareSize) * imageNumber
(467kB + 250kB) * 2 = 1234kB = 1.5MB
The result of 1.5MB leads to the S25FL016P with 16,777,216 Bits = 2MB.

Please refer to [2] (table 5-5, page 69) for detailed description of FPGA design memory consumption.

The reference HW design for a serial Flash (S25FL064P) is shown with a Xilinx Spartan 6 XC6SLX16 FPGA in [1] on page 38.

1.6 Ethernet

The hardware platform of the POWERLINK slave should include the Ethernet interface. In order to allow flexible topologies two Ethernet ports are recommended. IEEE 802.3 compliant Phys with RMII (Slave Mode) should be used.

Design Recommendation	
Data rate	**100 MBit/s**
Interface	**RMII**

The reference HW design for an Ethernet Phy (DP83630) is shown with a Xilinx Spartan 6 XC6SLX16 FPGA in [1] on page 5.
The following Ethernet Phys are recommended:

- NATIONAL DP83640/DP83630
- NATIONAL DP83848T

1.7 Clock Generation

The POWERLINK slave hardware should be equipped with a **50MHz (±50ppm)** clock source, which sources the FPGA and the Ethernet Phys.
The clock lines to the components must introduce the same delay for all clock connections.

The reference HW design for the clock generation (50MHz clock source and clock driver) is shown with a Spartan 6 XC6SLX16 FPGA in [1] on page 2.

1.8 Node Switches

In order to configure the POWERLINK CN, two node switches, introducing a hexadecimal digit each, provide a flexible solution for a quick change of the POWERLINK Node ID with a screw driver.

1.9 Interface

In order to gain access to the PDO data there are several interfaces possible.

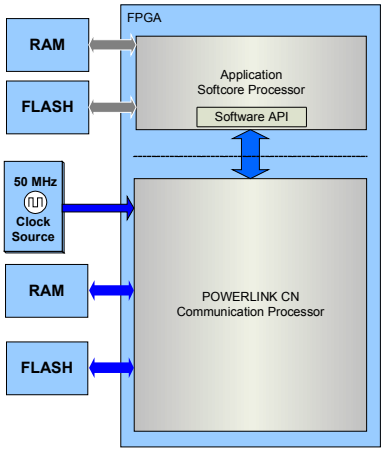

Fig. 2: Customer Application Running on FPGA Internal Soft-Core MCU

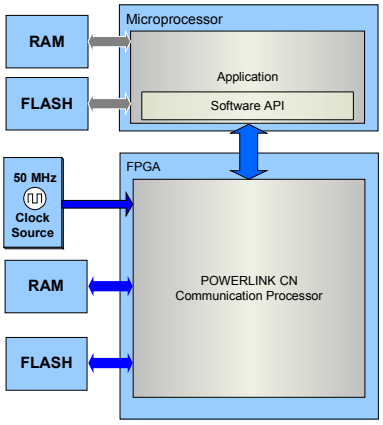

Fig. 3: Customer Application Running on External MCU

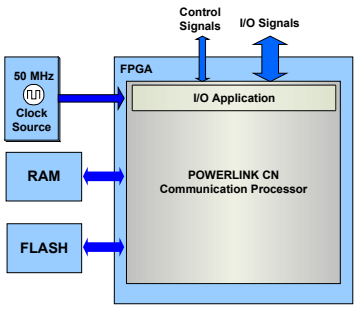

Fig. 4: Customer Accesses Only Cyclic Data via Digital I/O Interface

1. Customer application is running on the same FPGA with an additional FPGA internal CPU (soft-core) – see Fig. 2.
2. Customer application is running on a separate external MCU. The interface which provides the communication between the POWERLINK CN Communication Processor (PCP) and the external MCU could be e.g. SPI or an 8/16 Bit interface, as desired by the customer – see Fig. 3.

Information:

For users with FPGA knowledge it is possible to create their own interface IP-core in order to access the PCP. For the user, the PCP acts similar like an intelligent memory device then.

3. The simplest solution is a digital I/O interface which serves as PDO data access for both directions (TPDO, RPDO). This solution is fixed and not capable of any configuration during runtime – see Fig. 4.

1.9.1 SPI Slave Interface

The external application processor (AP) has the possibility to access e.g. PDO data via SPI. In this case the POWERLINK CN Communication Processor (PCP) acts as the SPI slave and the AP takes the SPI master role.
For the SPI interface only 5 signals (4 SPI and 1 IRQ – refer to Fig. 5) are necessary to interconnect the Application Processor and the FPGA. However, in order to enable further upgrades two GPIO signals are recommended!

Signal	Description	Direction[1]
SPI_CLK	SPI clock generated by SPI master	INPUT
SPI_SEL_n	SPI chip select (low active)	INPUT
SPI_MOSI	SPI Master Output to Slave Input	INPUT
SPI_MISO	SPA Master Input to Slave Output	OUTPUT
Sync IRQ	Interrupt request for synchronization	OUTPUT
GPIO(1:0)	General Purpose In-/Outputs	BIDIR

Tab. 1: SPI Interface Signals

1) The direction is seen from FPGA point of view.

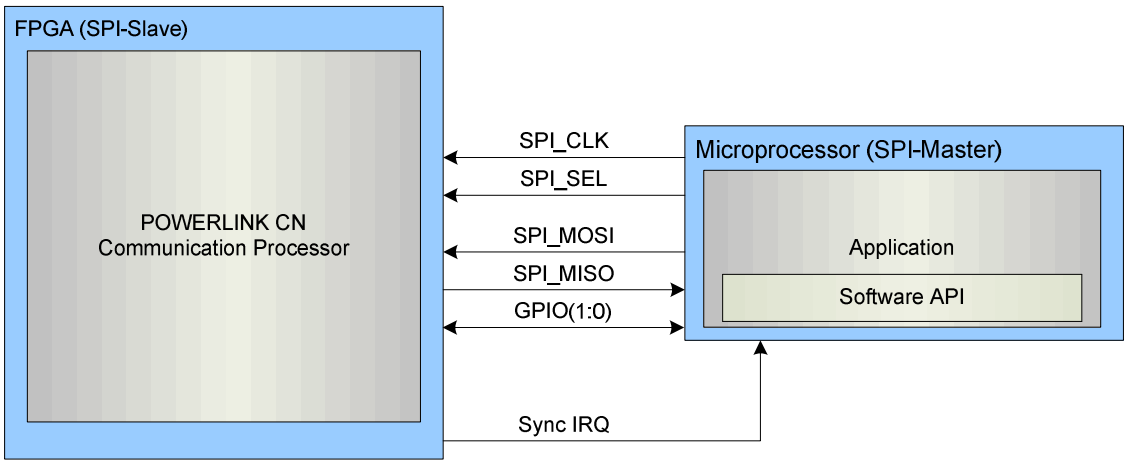

Fig. 5: Serial PCP (SPI Slave) to AP (SPI Master) Connection

1.9.1.1 Configuration

The SPI slave implements the following features:

- SPI Slave
- 8bit data
- Support of all four modes (CPOL = 0 or 1 and CPHA = 0 or 1)
- Shift direction: MSB first

1.9.1.2 Access

The communication via SPI requires coding the address and data into single SPI frames. Due to the high address range of the PDI the SPI core stores in total ten address bits (ADDR(14..5)) and reuse them as long as they are unchanged. The address bits 4 to 0 are transmitted before the final data transfer.

The protocol differs between two types of frames:

- Command Frame
- Data Frame

SPI allows full-duplex data transfer, however the SPI Slave PDI does not support that feature. The SPI Slave shifts out valid data only if a data transfer from SPI Slave to Master was initialised.

The POWERLINK FPGA Slave package is delivered with an SPI driver that implements the communication protocol.

1.9.1.3 Timing Specification

The PDI SPI Slave core implements all four modes as visualized in Fig. 6. After one data transfer the SPI Master may deassert the SPI select signal (SS) or start another transfer. Between two “SPI frames” the SPI Master should wait for one SPI Cycle (= period of SCK) at least.

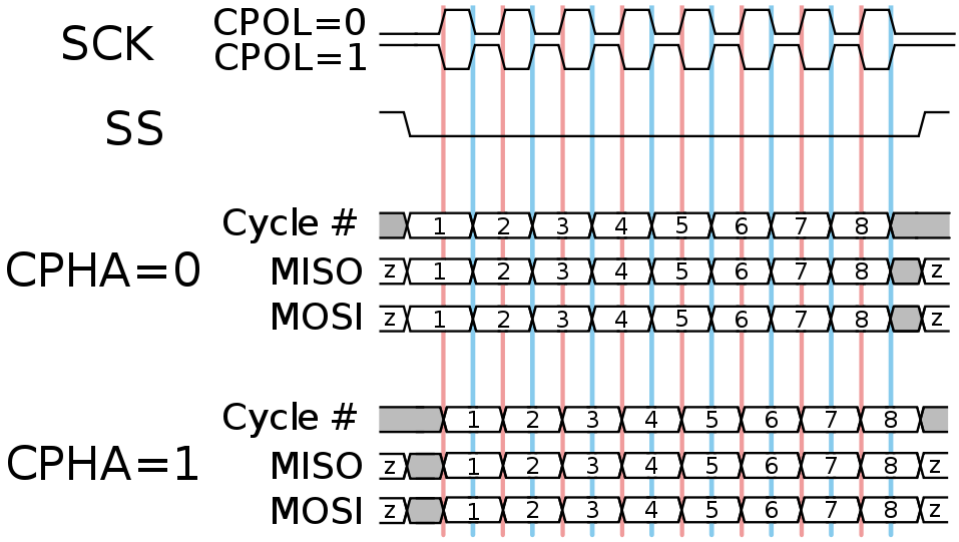

Fig. 6: SPI timing

Merit	Value		Comment
	Min	Max	
f_{CLK}	-	1MHz	SPI clock frequency is driven by the SPI Master. Maximum clock rate depends on PCB layout and might achieve a higher rate than specified.
t_{gap}	1µs	-	Time gap between SPI data frames. SPI Select (SS) may hold.

Tab. 2: Timing Specification of SPI MCU Interface

1.9.2 Asynchronous 8/16bit MCU Interface

For highest performance a parallel interface is recommended that uses a separate data- and address bus. The parallel connection can be configured (1.9.2.1) to transfer 8bit or 16bit data over the bidirectional data bus. The asynchronous 8/16bit MCU interface can be connected to many MCUs available on the market. Nevertheless it is essential to comply with the timing requirements listed in Tab. 4, since the asynchronous signals are synchronized inside the FPGA.

Signal	Description	Direction[2]
CS	Chip select	INPUT
WR	Write	INPUT
RD	Read	INPUT
BE	Byte Enable (only necessary for 16bit interface)	INPUT
ADDR	Address bus	INPUT
DATA	Data bus	BIDIR
ACK	Acknowledge signal (optional)	OUTPUT
Sync IRQ	Interrupt request for synchronization	OUTPUT
GPIO(1:0)	General Purpose In-/Outputs	BIDIR

Tab. 3: Asynchronous MCU Interface Signals

2) The direction is seen from FPGA point of view.

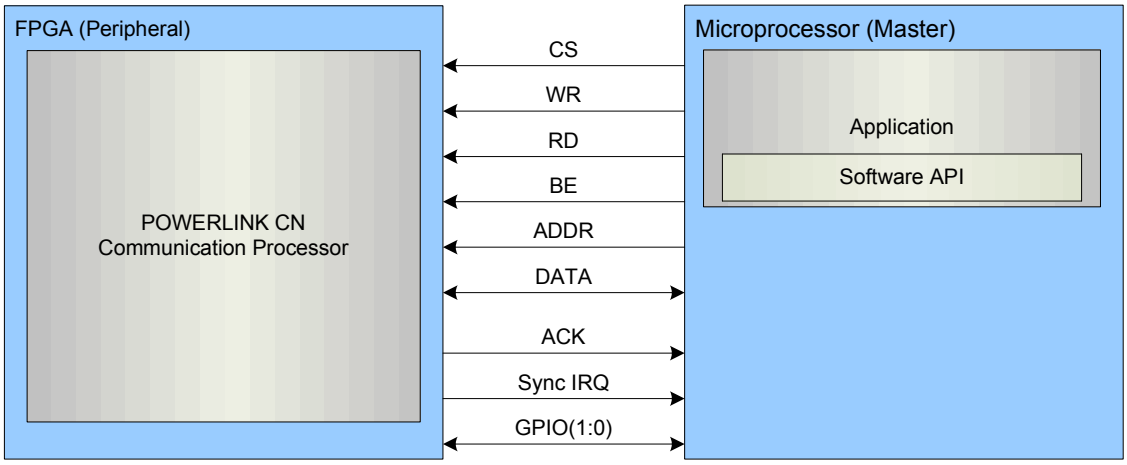

Fig. 7: Generic Parallel PCP to AP Connection

1.9.2.1 Configuration

The parallel interface has to be configured to either 8 or 16bit in the development environment. Every configuration includes the common control signals:

- Chip select (CS)
- Write strobe (WR)
- Read strobe (RD)
- ACK (optional)
- Interrupt request (IRQ)

For the 8bit configuration (Fig. 8) the bidirectional data bus decreases to 8 signal lines and omits the Byte Enable signals (BE).

The 16bit configuration (Fig. 9) requires a data bus of 16 signal lines and the Byte Enable signals (BE). The Least Significant Bit of the address bus ADDR(0) is omitted.

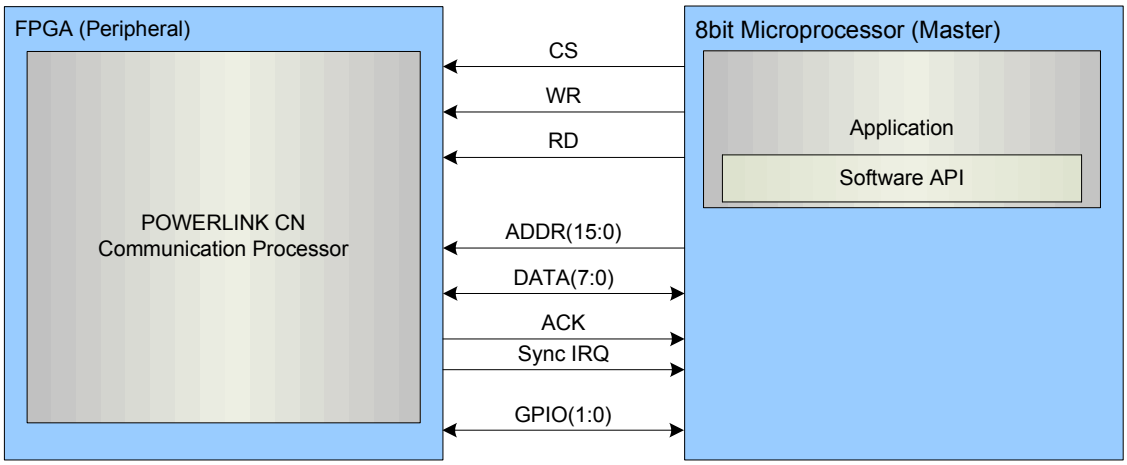

Fig. 8: 8bit Parallel PCP to AP Connection

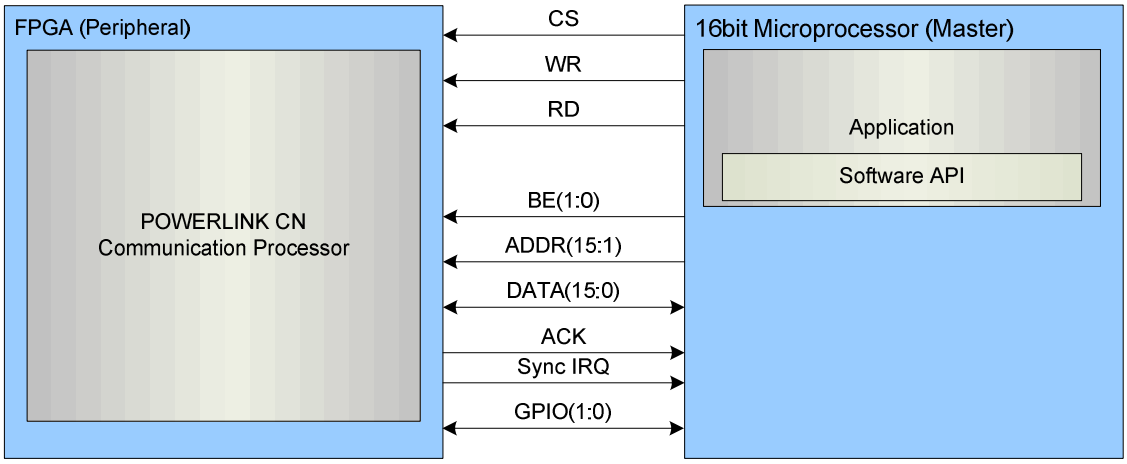

Fig. 9: 16bit Parallel PCP to AP Connection

1.9.2.2 Write Access

The timing specification of a write access is shown in Fig. 10.
The CS signal has to be asserted with the other control signals (BHE, BLE and WR) or before (1). The address and BHE and BLE have to be set with the WR signal. The write signals have to be set for at least the Write Pulse Time (t_{PWR}) to allow the address and BE signals to propagate into the IP-Core. The AP may hold the signals to insert wait-states.
The falling edge of the WR signal (2) latches the data on the data bus. Setup and Hold Data time depend on the fitter results! The AP must hold the valid address and BE signals for a certain time (t_{HA}) before starting the next write (3a) or read (3b) access.
The optional ACK signal is asserted by the FPGA after a delay (t_{WAD}).

1.9.2.3 Read Access

The timing specification of a read access is shown in Fig. 11.
The CS signal has to be asserted with the other control signals (BHE, BLE and RD) or before (1). After the address access time (t_{AA}) the data bus is driven by the FPGA with the valid data (2). The AP may hold the signals to insert wait-states.
After the deassertion of the RD signal the valid data is hold for t_{OHA} on the data bus. Afterwards the FPGA changes the data bus to inputs (3). Note that the next write (4a) or read (4b) access must not start before the end of t_{RNA}.
The optional ACK signal is asserted synchronously to the valid read data on the data bus.

1.9.2.4 Timing Specification

Symbol	Value		Comment
	Min	Max	
t_{SC}	0ns	-	The CS signal has to be asserted before or with write or read signals.
t_{HC}	0ns	-	The CS signal has to be deasserted after or with write or read signals.
t_{HA}	40ns	-	The valid address has to be hold before the next write or read access.
t_{PWR}	20ns	-	Write pulse Note: The WR signal can be hold for a certain time to insert wait-states.

t_{SD}	X[3]	-	Data Setup to Write End
t_{HD}	X[3]	-	Data Hold from Write End
t_{RNA}	40ns	-	After a read access the next write or read has to be asserted after a delay.
t_{AA}	60ns	80ns	Address access time after the data bus is driven with valid data.
t_{OHA}	20ns	40ns	Valid output data to be held on the data bus (before changing to HIGH Z).
t_{WAD}	40ns	60ns	ACK signal assertion after Write END
t_{AP}	20ns	-	ACK signal assertion duration

Tab. 4: Timing Specification of Asynchronous 8/16bit MCU Interface

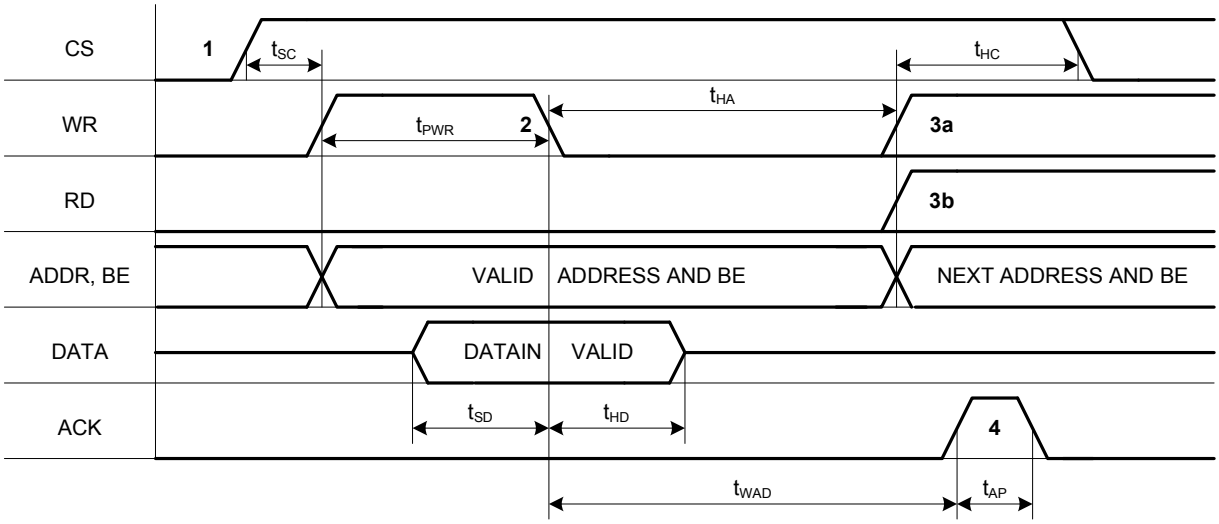

Fig. 10: Write Access Timing

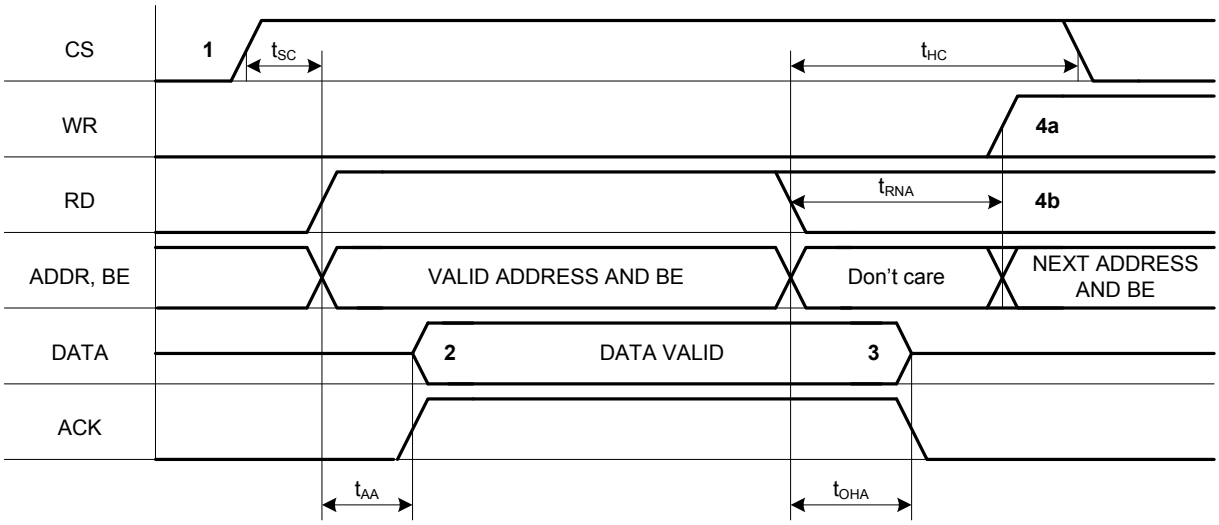

Fig. 11: Read Access Timing

[3] The parameter depends on the Fitter result.

1.9.3 Digital I/O Interface

The digital I/O-interface supports 4 Bytes of digital I/O signals. Each byte can be assigned as input or output, which is defined by the logical levels of PORTCNFA/B/C/D. These signals will be captured at start up by the PCP.

Pin	Name		Direction[4]	Description
1	I/O1	PORT A	BIDIR	Digital Input/Output 1
2	I/O2		BIDIR	Digital Input/Output 2
3	I/O3		BIDIR	Digital Input/Output 3
4	I/O4		BIDIR	Digital Input/Output 4
5	I/O5		BIDIR	Digital Input/Output 5
6	I/O6		BIDIR	Digital Input/Output 6
7	I/O7		BIDIR	Digital Input/Output 7
8	I/O8		BIDIR	Digital Input/Output 8
9	I/O9	PORT B	BIDIR	Digital Input/Output 9
10	I/O10		BIDIR	Digital Input/Output 10
11	I/O11		BIDIR	Digital Input/Output 11
12	I/O12		BIDIR	Digital Input/Output 12
13	I/O13		BIDIR	Digital Input/Output 13
14	I/O14		BIDIR	Digital Input/Output 14
15	I/O15		BIDIR	Digital Input/Output 15
16	I/O16		BIDIR	Digital Input/Output 16
17	I/O17	PORT C	BIDIR	Digital Input/Output 17
18	I/O18		BIDIR	Digital Input/Output 18
19	I/O19		BIDIR	Digital Input/Output 19
20	I/O20		BIDIR	Digital Input/Output 20
21	I/O21		BIDIR	Digital Input/Output 21
22	I/O22		BIDIR	Digital Input/Output 22
23	I/O23		BIDIR	Digital Input/Output 23
24	I/O24		BIDIR	Digital Input/Output 24
25	I/O25	PORT D	BIDIR	Digital Input/Output 25
26	I/O26		BIDIR	Digital Input/Output 26
27	I/O27		BIDIR	Digital Input/Output 27
28	I/O28		BIDIR	Digital Input/Output 28
29	I/O29		BIDIR	Digital Input/Output 29
30	I/O30		BIDIR	Digital Input/Output 30
31	I/O31		BIDIR	Digital Input/Output 31
32	I/O32		BIDIR	Digital Input/Output 32

4) Table Note: The direction is seen from FPGA point of view.

33	PORTCNFA	INPUT	Port A: 0 = In, 1 = Out
34	PORTCNFB	INPUT	Port B: 0 = In, 1 = Out
35	PORTCNFC	INPUT	Port C: 0 = In, 1 = Out
36	PORTCNFD	INPUT	Port D: 0 = In, 1 = Out
37	OP	OUTPUT	1 = CN is operational

Tab. 5: Digital I/O Interface Signals

1.9.3.1 Latch Timing Specification

The Digital I/O interface provides for each input byte a latch signal, which is level sensitive (high). This feature is useful when connecting an ADC or similar chip to the FPGA.
If the latch functionality is not used, simply tie the latch input to high (within FPGA or external).
Fig. 12 shows the timing diagram of the latch functionality. Tab. 6 defines the minimum high pulse of the latch signal. Please note that only the last stable input data (in Fig. 12 INPUT DATA C) is stored after the latch pulse. Any other input data (in Fig. 12 INPUT DATA B) will be lost!

Symbol	Value		Comment
	Min	Max	
t_{LP}	20ns	-	Latch high pulse
t_{DV}	20ns	-	Valid input data

Tab. 6: Timing Specification of the Latch functionality of Digital I/O

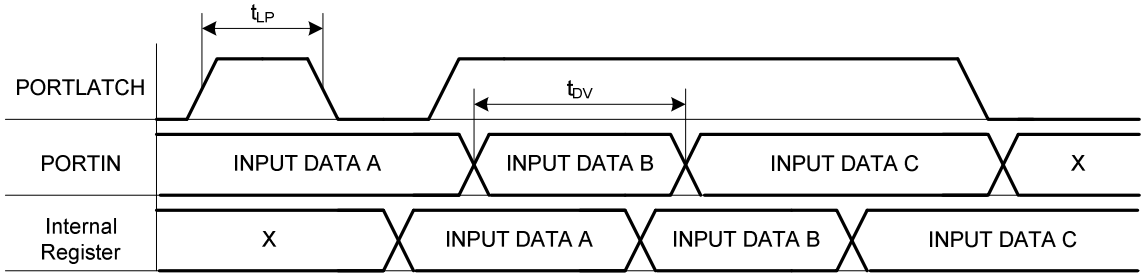

Fig. 12: Latch Timing

1.9.4 AXI/PLB Slave Interface

The AXI or PLB slave interface is necessary for designs where the PCP and the AP processor in located in one Xilinx FPGA.

Please refer to [3] or [4] for more information about Xilinx internal bus systems.

1.10 Debugging and FPGA Programming

For debugging the FPGA design in an early state of development, and downloading the FPGA configuration, a JTAG interface is recommended. This is not mandatory for the final product design, although it might also provide a way to initially program the serial FLASH memory “In System”. In addition a USB UART can be included to see faster debug output from one of your processors.

2 Softcores

The POWERLINK slave design requires the following soft-cores:

Design Recommendation		Provider
CPU	Microblaze® (second Microblaze® for application is optional)	Xilinx
MAC Layer	POWERLINK IP-Core	Non-Proprietary
Controller & Interfaces	e.g. Memory Controller, JTAG UART etc.	Xilinx, Evaluation board manufacturer
Node switches, POWERLINK LED	GPIO	Xilinx

Some additional notes:

- **Microblaze**® soft-core processor (second Microblaze® is optional)
  Depending on the desired design the application processor might be FPGA external or internal. Either way one Microblaze® is mandatory for processing the openPOWERLINK protocol stack.

- **POWERLINK IP-Core containing:**
  1. **openMAC**
     This soft-core is non-proprietary (means free of charge). It implements the Ethernet MAC layer and provides additional features useful for POWERLINK.

  2. **openHub**
     This soft-core is non-proprietary. It implements an inside FPGA Hub. Using two Ethernet Phys with an optional Hub allows flexible topologies.

  3. **Process Data Interface (PDI)** for processor interconnection.

- Further necessary IP-cores come with the evaluation board package and/or from Xilinx

3 Definitions and Abbreviations

AP	Application Processor
CN	POWERLINK Controlled Node
FPGA	Field Programmable Gate Array
PCP	Powerlink Communication Processor
PDI	Process Data Interface
PDO	Process Data Object
SPI	Serial Peripheral Interface
DSP	Digital Signal Processor
MCU	Microcontroller Unit
CPU	Central Processing Unit
DPRAM	Dual Ported RAM
SRAM	Static RAM
RAM	Random Access Memory
IRQ	Interrupt Request

4 Reference

[1] “POWERLINK S6 Board schematic” V1B
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[2] “Spartan-6 FPGA Configuration, V2.3” July 2011
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[3] “PLB v3.4 and OPB to PLB v4.6 System and Core Migration User Guide”, V1.2, December 2007
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